

Starload GPU board Schematics Skylake-U


2016/02/18

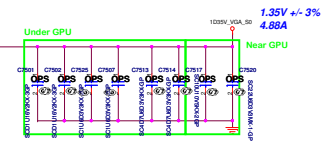
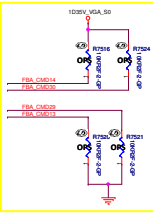
REV : A00

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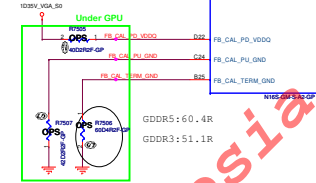
IO board

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
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GPU Package Type	Capacitor Type	Footprint	Population	Location	
GB2B-64/ GB2-64 GDDR5	0.1 μ F	X7R 0402	2	2	Under GPU
	1 μ F	X7R 0603	2	2	Under GPU
	4.7 μ F	X6S 0603	2	2	Under GPU
	10 μ F	X5R 0805	1	1	Hear GPU
	22 μ F	X5R 0805	1	1	Hear GPU



GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB3B-256	GPCPLL_AVDD0/I+ LVX_PLLVDD+ FB_PLL_DLL_AVDD0/I	0.1 μ F X7R	0402	5	Under GPU
		22 μ F X5R	0805	1	Near GPU
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU

Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

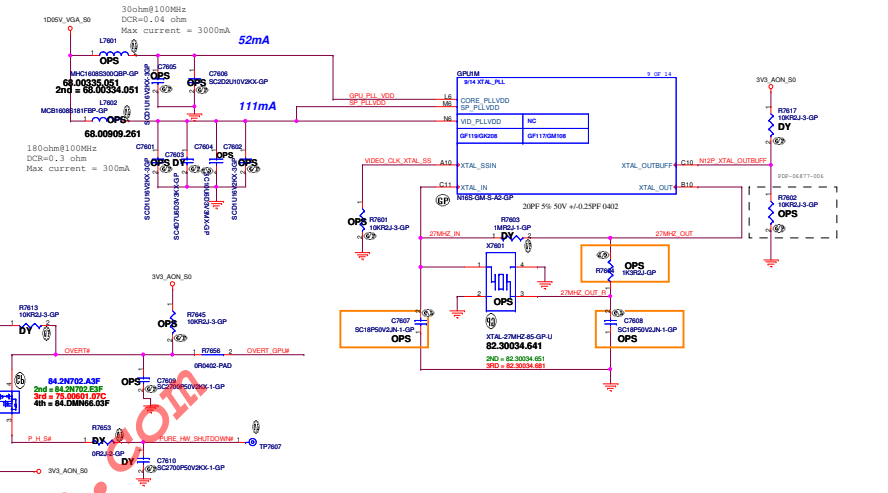
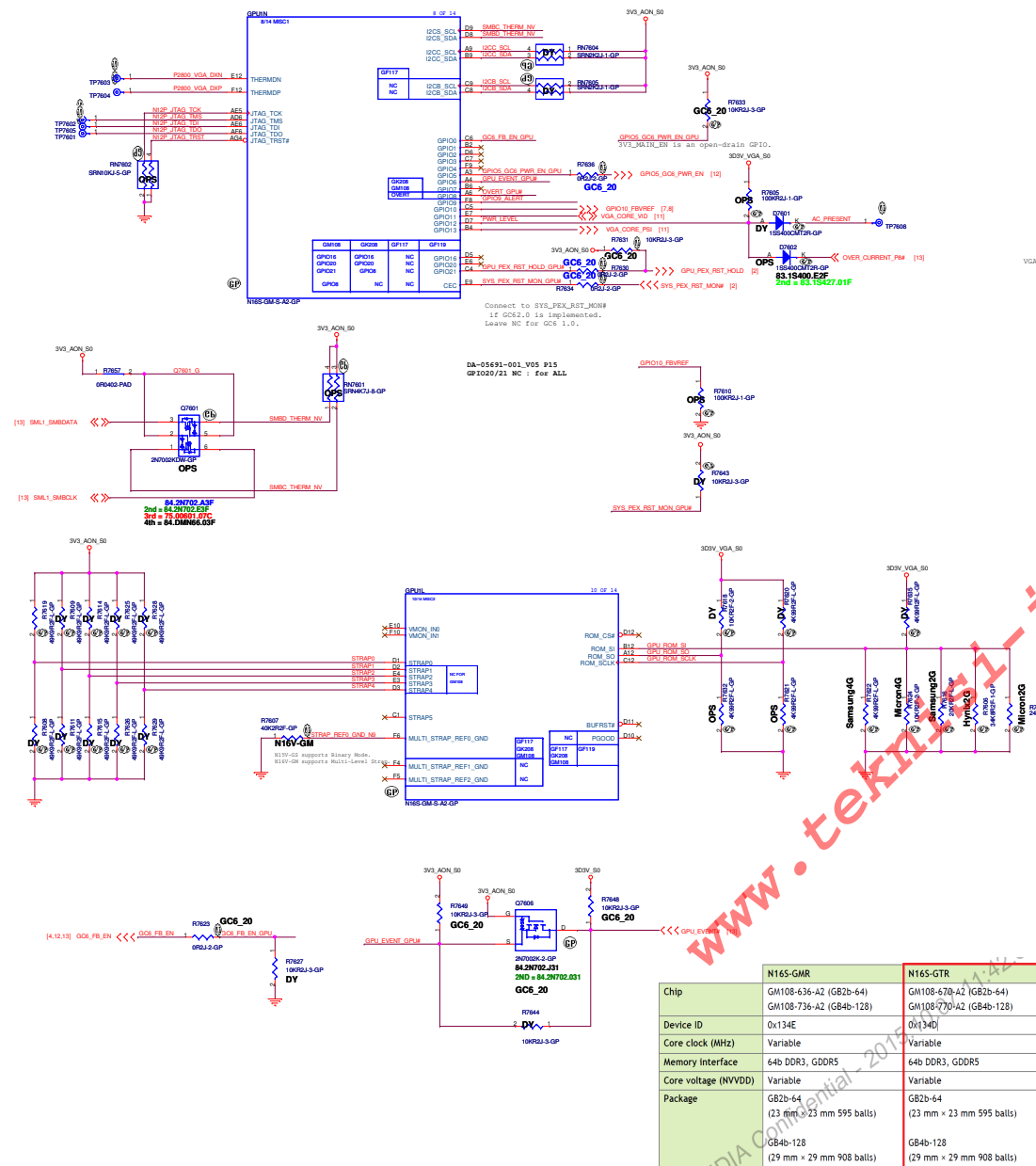


Table 16. N165-GMR /-GTR GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	256Mx16	Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
		128Mx32	Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
		128Mx32	Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
		256Mx32	Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
		256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
		512Mx16	Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
			Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready

Note: For N165-GMR/-GTR, the maximum allowable memory case temperature is 85 °C.

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AOH and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AOH and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				

Table 15-2. Resistance Mapping to Hex Values

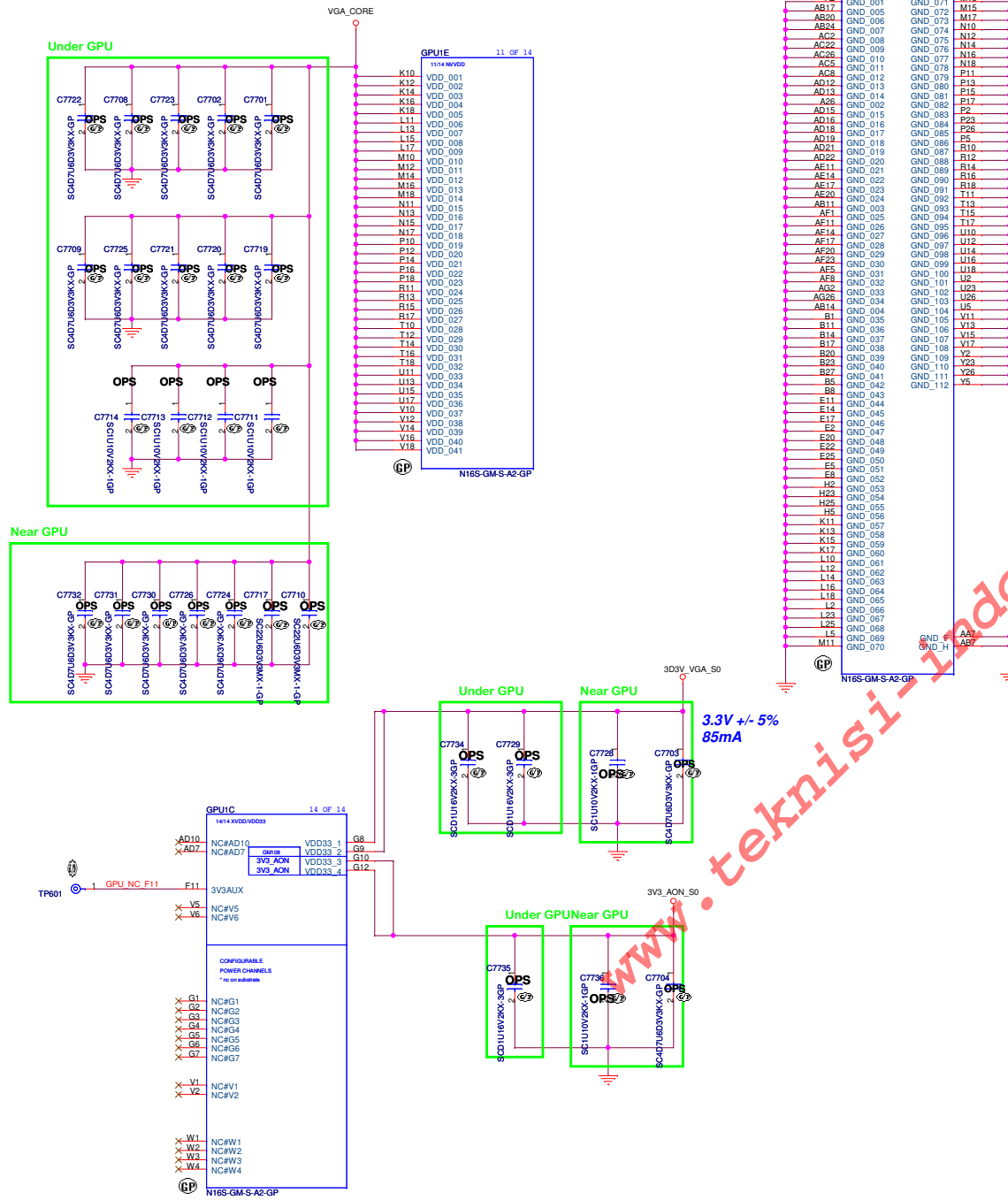
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

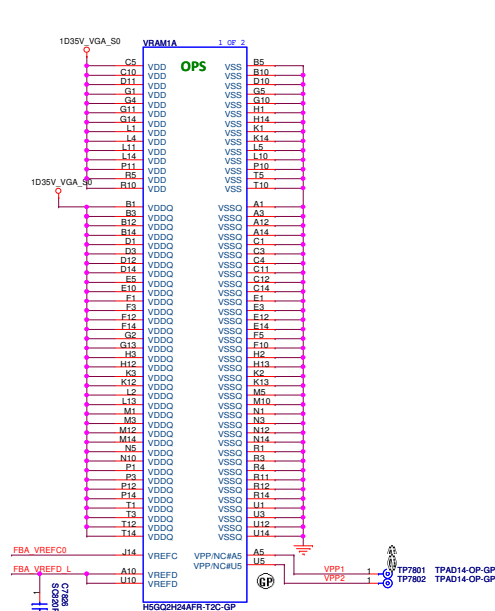
STRAP PIN MODE TABLE

PIN NAME	GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping	GF117: BINARY STRAPS
STRAP0	USER[3:0]	RAM_CFG[0]
STRAP1	3GIO_PADCFG_ADR[3:0]	RAM_CFG[1]
STRAP2	PCI_DEVVID[3:0]	RAM_CFG[2]
STRAP3	SOR[3:0]_EXPOSED	RAM_CFG[3]
STRAP4	RESERVED, PCIE_SPEED_CHANGE_GNE3, PCIE_MAX_SPEED, DP_PLL_VDD_33V	PCIE_MAX_SPEED
ROM_SCLK	PCIDEVID[4], SUB_VENDOR, PCIDEVID[5], PEX_PLL_EN_TERM	SMB_ALT_ADDR
ROM_SI	RAMCFG[3:0]	SUB_VENDOR
ROM_SO	FB[1], FB[0], SMB_ALT_ADDR, VGA_DEVICE	VGA_DEVICE

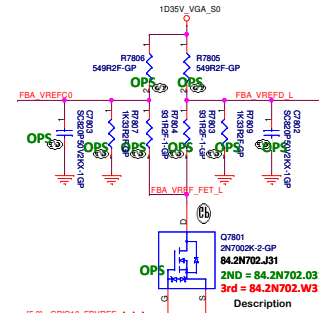
	N165-GMR	N165-GTR
Chip	GM108-636-A2 (GB2B-64) GM108-736-A2 (GB4B-128)	GM108-670-A2 (GB2B-64) GM108-770-A2 (GB4B-128)
Device ID	0x134E	0x134D
Core clock (MHz)	Variable	Variable
Memory interface	64b DDR3, GDDR5	64b DDR3, GDDR5
Core voltage (NVDD)	Variable	Variable
Package	GB2B-64 (23 mm × 23 mm 595 balls) GB4B-128 (29 mm × 29 mm 908 balls)	GB2B-64 (23 mm × 23 mm 595 balls) GB4B-128 (29 mm × 29 mm 908 balls)

Main Func = dGPU



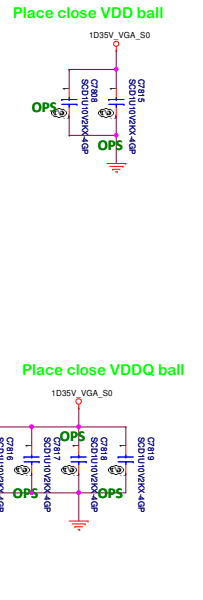
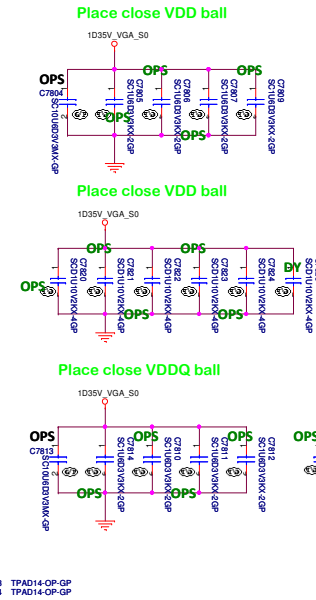
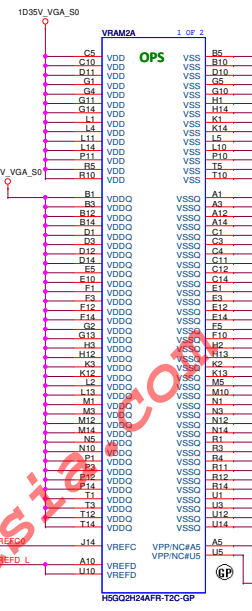


Frame Buffer Partition A-Lower Half

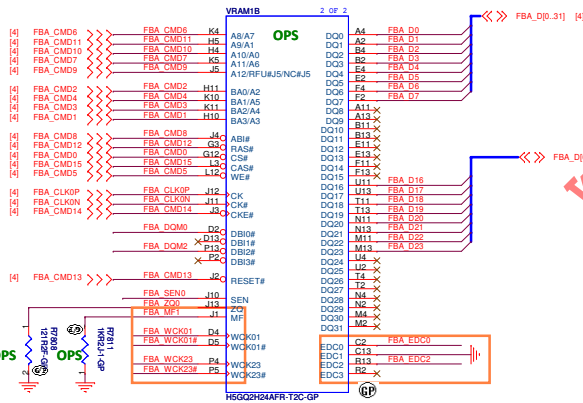


FBVREF Termination

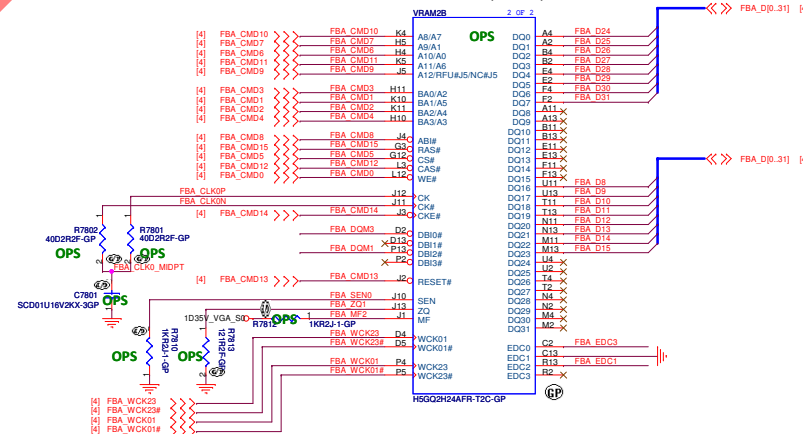
Type	FBVREF%	Voltage	GPU GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



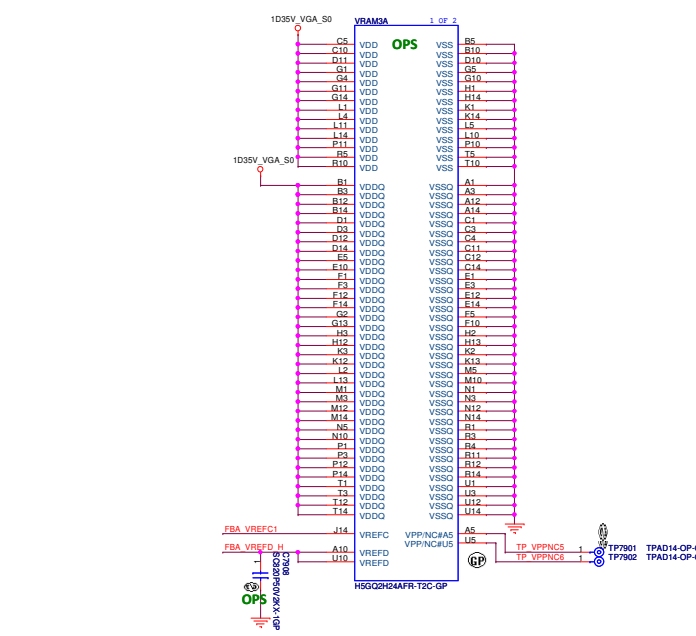
Normal(MF=0)



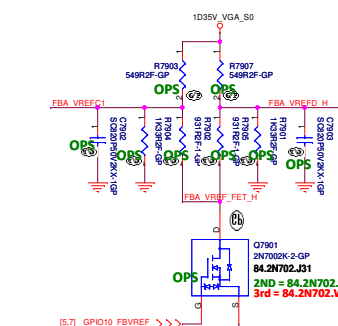
Mirrored(MF=1)



<Core Design>

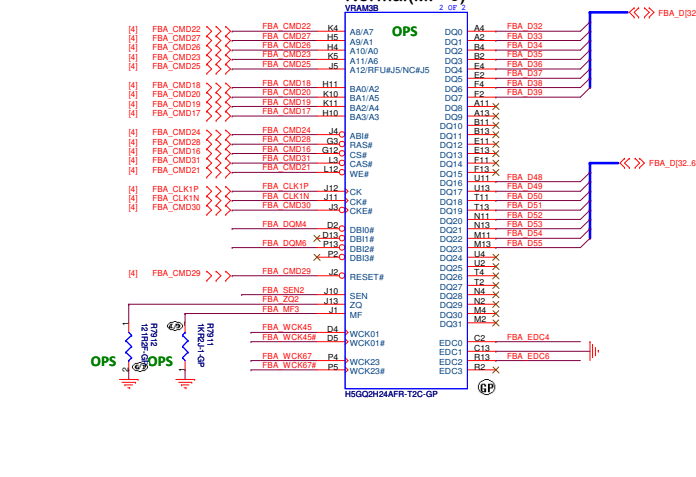
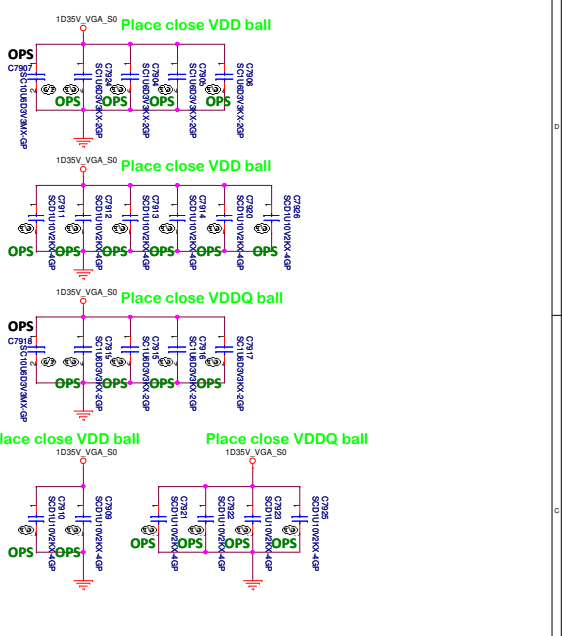
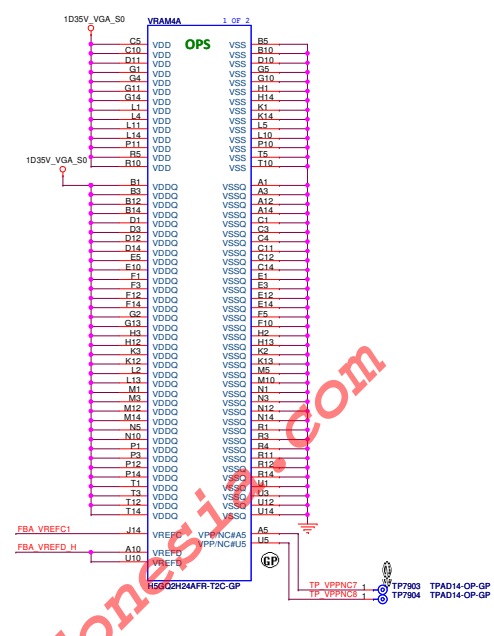


Frame Buffer Partition A-Upper Half

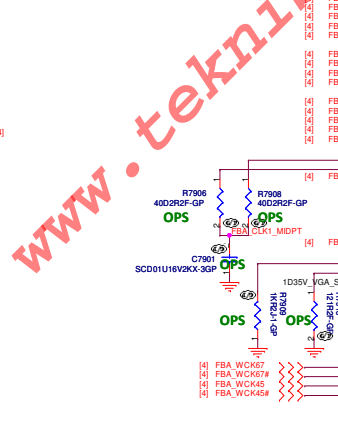


FBVREF Termination

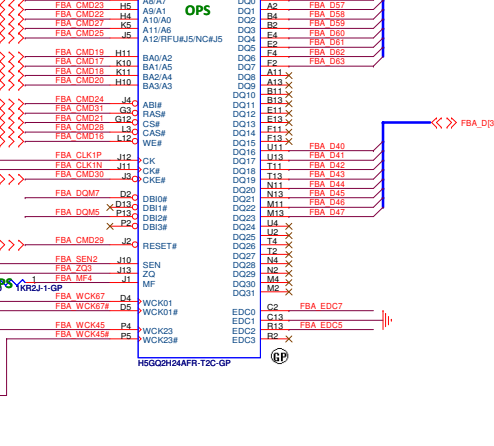
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Normal(MF=0)



Mirrored(MF=1)




Main Func = dGPU

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<Core Design>



Wistron Corporation
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Title

GPU-VRAM7,8 (4/4)

Size
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Starload SKL-U

Rev
A00

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N16V_GM_B1
Config B

Design Current=33.5A
56.65A <OCP< 66.7A

Component Value	N15V-GM-S Config D	N16V-GM-B1 Config B
R1 (PR8223)	27K 64.27025,60L	20K 64.20025,60L
R2 (PR8206)	7.5K 64.75015,60L	20K 64.20025,60L
R3 (PR8209)	0 63.800014,10L	2K 64.20015,60L
R4+R5 (PR8209)	7.5K 64.75015,60L	1.8K 64.18023,60L
C (PC8223)	5.60F 78.56222,28F	2.70F 78.27224,28F

78.56222,28F: OMS REASON: 50V is more popular, change to 78.56224,28F

For tuning VGA_CORE sequence.

I/P cap: 10U 25V K0805 X5R/ 78.10622,51L
Inductor: CHIP CHORE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S: SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm@4.5Vgs/ 84.SRA06.037

Design Current=33.5A
79.5A <OCP< 95.4A

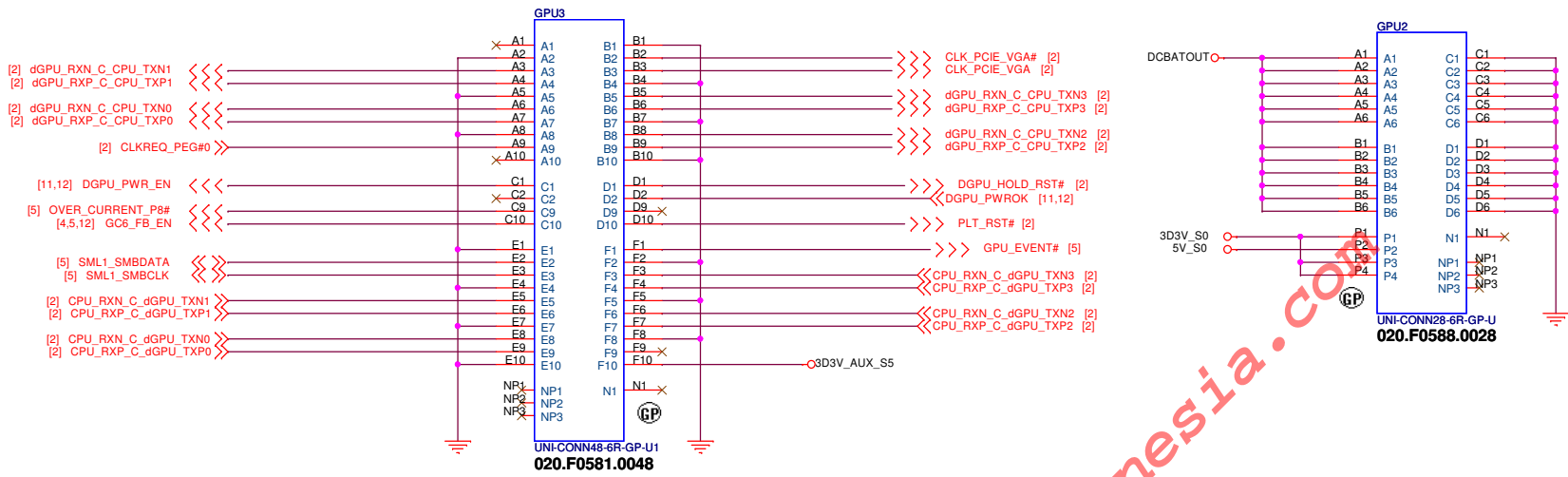
N16V_GM_B1
Config B

Table 1. PWM-VID Spec and Component Values

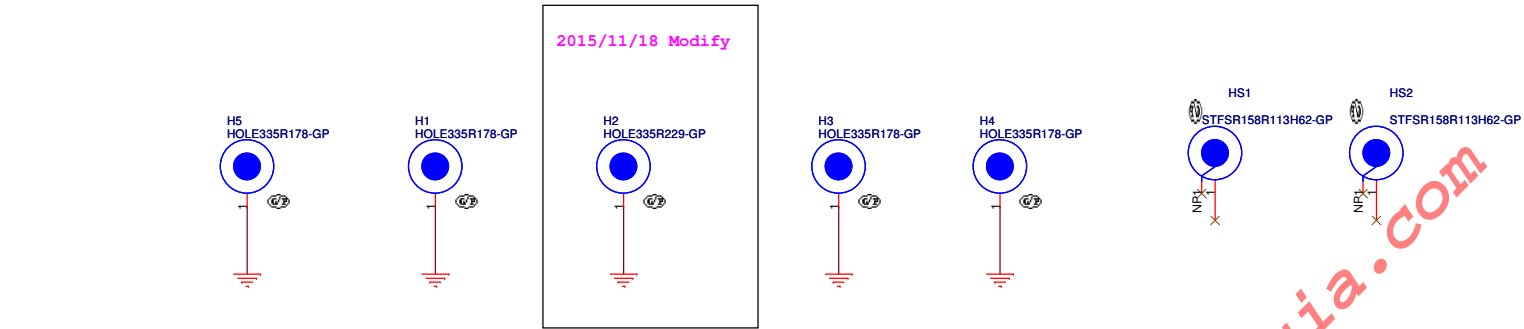
PWM-VID Specification		Config A	Config B
Vmin	V	0.6	0.6
Vmax	V	1.2	1.2
Vboot	V	0.875	0.9
Voltage Step Vstep	mV	6.25	6.25
Number of Voltage Levels H level		96	96
PWM Frequency F _{PWM}	Hz	1.125	1.125
PWM Minimum Pulse Width T _{min}	ns	9.26	9.26
VID Transient Time T	us	<100	<100
Component Value			
R1 (1%)	KQ	39	20
R2 (1%)	KQ	39	20
R3 (1%)	KQ	1.5	2
R4 (1%)	KQ	30	18
R5 (1%)	KQ	1.5	0
C	nF	1.5	2.7

<Core Design>

Main Func = Connector



Main Func = UnusedParts



Main Func = EMICapacitors

